IN THE CLAIMS

A listing of the claims presented in this patent application appears below. This listing replaces all prior versions and listing of claims in this patent application.

1-8. (Cancelled)

9. (Currently Amended) A programmable logic device comprising an array of programmable logical elements, said programmable logic device characterized in that said logical elements include:

first logical elements having a predetermined logic; and

second logical elements having the same logic as said first logical elements but having an upper limit of operating speed of a transistor in the second logical elements designed to be lower than that of said first logical elements.

10. (Currently Amended) The programmable logic device according to claim 9, wherein each of said second logical elements uses transistors higher in threshold voltage compared with transistors used in each of said first logical elements,

wherein the first and second logical elements are allocated based on processes of an application program.

11. (Currently Amended) The programmable logic device according to claim 9, wherein said second logical elements have a transistor size ~~layout structure~~ different from that of said first logical elements.

12. (Previously Presented) The programmable logic device according to claim 9,

wherein the first logical elements are operated by a clock signal with a first clock frequency; and

said second logical elements are operated by a clock signal with a second clock frequency lower than said first clock frequency.

13. (Previously Presented) The programmable logic device according to claim 9, wherein said first logical elements are arranged collectively in one place.

14. (Previously Presented) The programmable logic device according to claim 13, wherein said first logical elements are arranged in a center portion of said programmable logic device; and

said second logical elements are arranged in a peripheral portion of said programmable logic device with respect to the region where said first logical elements are arranged.

15. (Previously Presented) The programmable logic device according to claim 13, wherein:

said second logical elements are arranged in a center portion of said programmable logic device; and

said first logical elements are arranged in a peripheral portion of said programmable logic device with respect to the region where said second logical elements are arranged.

16. (Currently Amended) A method of designing a programmable logic device formed from an array of programmable logical elements, said method characterized by comprising the steps of:

designing first logical elements having a predetermined logic; and

designing second logical elements having the same logic as said first logical elements but having an upper limit of operating speed of a transistor in the second logical elements designed to be lower than that of said first logical elements.